BATTERY PACK SECURITY AND AUTHENTICATION IC FOR PORTABLE APPLICATIONS (bqSECURE™)

FEATURES

- **Provides Authentication of Battery Packs Through a Programmable CRC With a 96-bit Unique Device ID**
- **16 Bytes of User-Programmable Nonvolatile Memory**
- **12.5 KV IEC ESD Protection on HDQ Input**
- **Internal Time-Base Eliminates External Crystal Oscillator**
- **Low-Power Operating: <30 μA**
- **Single-Wire HDQ Interface**
- **Powered Directly From the Communication Bus**
- **Pass-Through HDQ Version Supports Existing Packs With Gas Gauges**

- **Small 5-Pin SC 70 package**

APPLICATIONS

- **Cellular Phones**
- **PDA and Smart Phones**
- **MP3 Players**
- **Digital Cameras**
- **Internet Appliances**
- **Handheld Devices**

DESCRIPTION

The bq26150 provides a method to authenticate battery packs, ensuring that only packs manufactured by authorized sub-contractors are used in the end application. The bq26150 uses a 96-bit unique device ID, device unique 16-bit seed, and a 16-bit device specific CRC to provide security. The device ID, CRC seed, and CRC polynomial coefficients are stored securely in each bq26150 device, allowing the host to authenticate each pack.

The bq26150 communicates to the system over a simple one-wire, bidirectional serial interface. The 5 kbits/s HDQ bus interfaces reduces communications overhead in the external microcontroller. The bq26150 also uses the HDQ bus to charge an external capacitor that provides power to the bq26150.
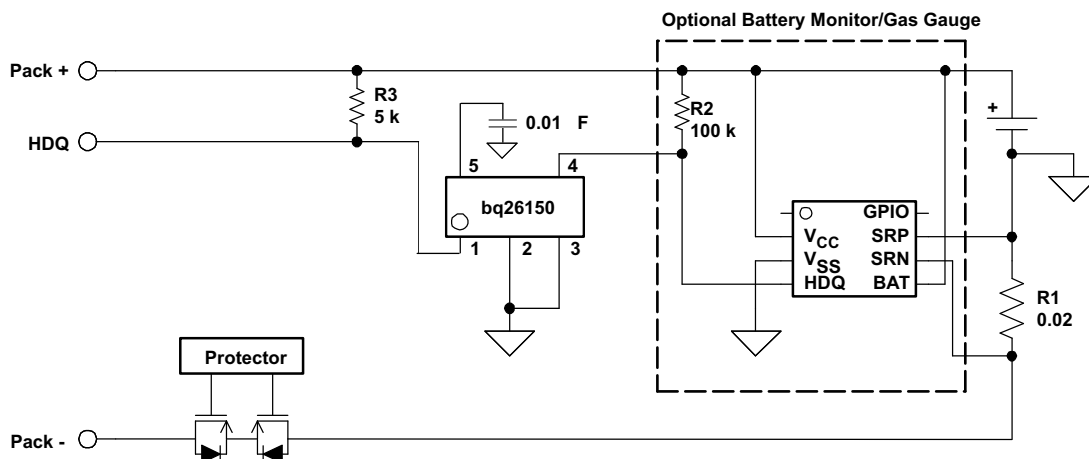
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TYPICAL APPLICATION

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T_A	PACKAGE	PART NUMBER
−20°C to 70°C	5-Lead SC 70	bq26150

ABSOLUTE MAXIMUM RATINGS[1]

		UNIT
V_{SS}	Supply voltage (HDQ with respect to V_{SS})	−0.3 V to 7.7 V
V_I	Input voltage (HDQP with respect to V_{SS})	−0.3 V to 7 V
I_O	Output current (HDQ and HDQP)	5 mA
T_A	Operating free-air temperature range	−20°C to 70°C
T_{stg}	Storage temperature range	−65°C to 150°C
T_J	Junction temperature range	−40°C to 125°C
	Lead temperature (soldering, 10 sec)	300°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
	Supply voltage, HDQ pull-up	2.5		5	V
T_J	Operating free-air temperature range	−20		70	°C

ELECTRICAL CHARACTERISTICS

All parameters over recommended operating temperature and supply voltage range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_I	Input capacitance	HDQ		400		pF
t_{d1}	Power up communication delay	Power capacitor charge time		100		ms
I_{CC}	V_{CC} current	$V_{CC} > V_{CC(min)}$		20	30	µA
$V_{(POR)}$	POR threshold	Low-to-high			1.5	V
	Nonvolatile memory programming voltage		7.0		7.7	V
	Nonvolatile memory programming supply current	−40°C and V_{CC} = 2.75 V			308	µA

HDQ AND HDQP PINS

over recommended operating temperature and supply voltage range (unless otherwise noted)

| PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage		1.8			V
V_{IL}	Input low voltage				0.7	V
I_{OL}	Output low sink current	V_{OL} = 0.4 V			1	mA

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STANDARD SERIAL COMMUNICATION (HDQ) TIMING

over recommended operating temperature and supply voltage range (unless otherwise noted) See Figure 1

|	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Power up delay	Power capacitor charge time		100		ms
$t_{(B)}$	Break timing		190			µs
$t_{(BR)}$	Break recovery		40			µs
$t_{(CYCH)}$	Host bit window		190			µs
$t_{(HW1)}$	Host sends 1		0.5		50	µs
$t_{(HW0)}$	Host sends 0		86		145	µs
$t_{(RSPS)}$	bq26150 to host response		190		320	µs
$t_{(CYCD)}$	bq26150 bit window		190		250	µs
$t_{(DW1)}$	bq26150 sends 1		32		50	µs
$t_{(DW0)}$	bq26150 sends 0		80		145	µs
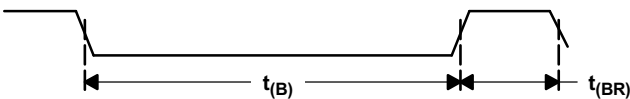
(a) Break and Break Recovery Timing;
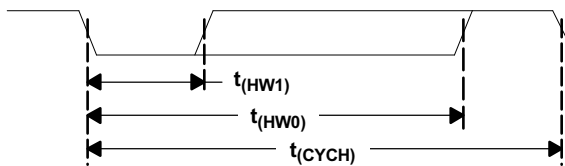
(b) Host Transmitted Bit Timing;
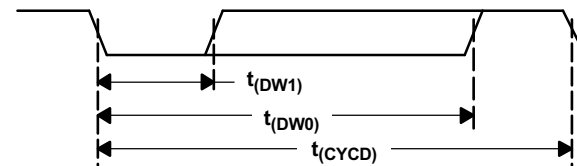
(c) bq26150 Transmitted Bit Timing;
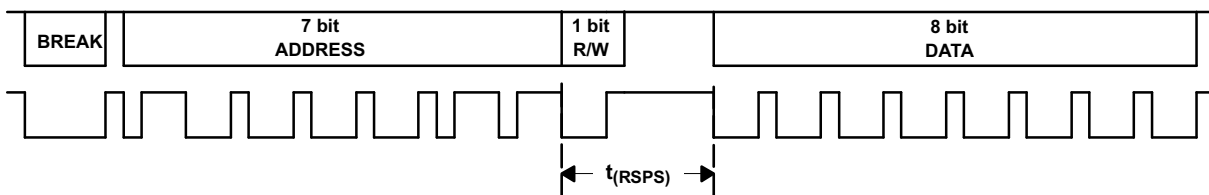
(d) bq26150 to Host Response Timing
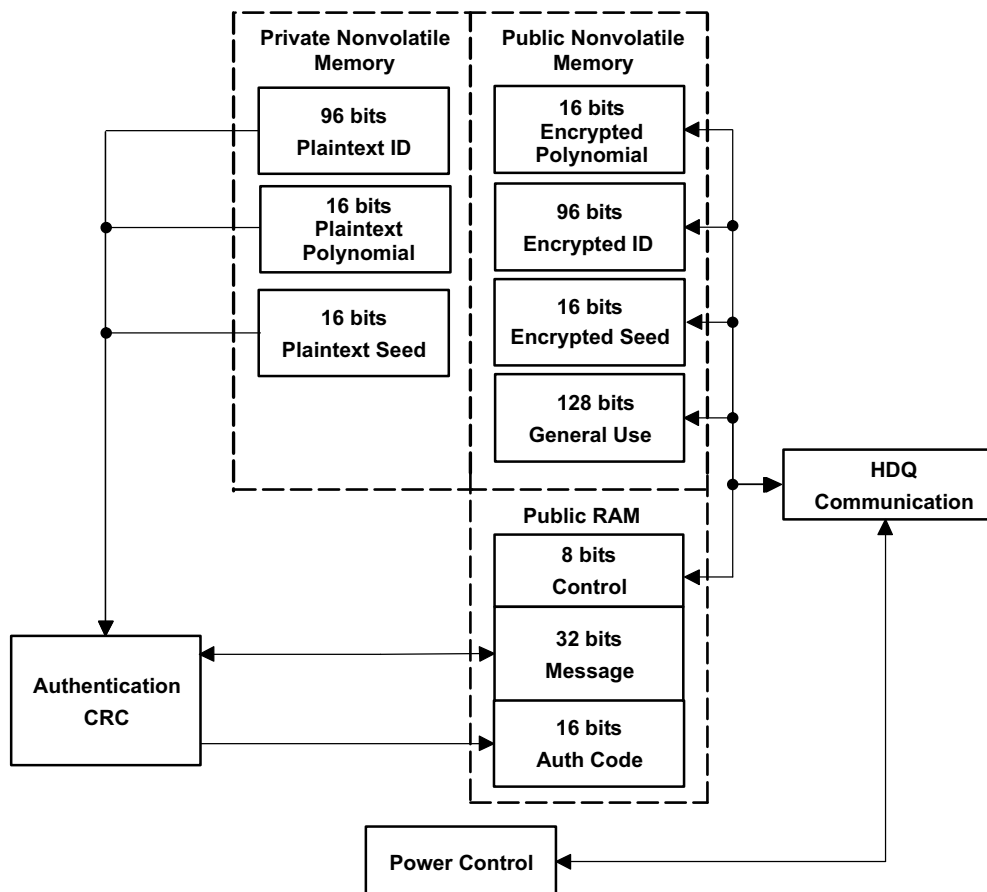
Figure 1. HDQ Bit Timing Diagrams

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PIN ASSIGNMENT

```
    PWR        HDQP

     5          4


     1    2     3

    HDQ  V_SS  V_SS
```
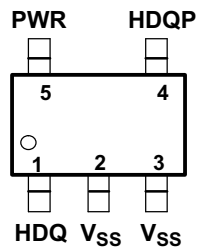
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
HDQ	1	I/O	Single-wire HDQ interface to host
VSS	2, 3	I	Ground
HDQP	4	I/O	Single-wire HDQ interface to 2nd HDQ device
PWR	5	I/O	Power capacitor

FUNCTIONAL BLOCK DIAGRAM

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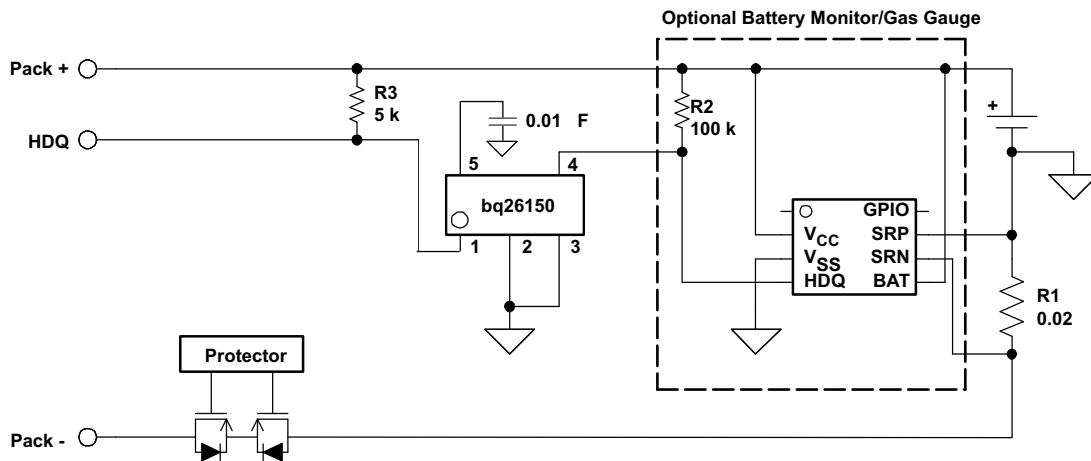## APPLICATION INFORMATION

Figure 2. Typical Application Circuit

FUNCTIONAL DESCRIPTION

The bq26150 provides a simple and cost effective method to authenticate battery packs for end equipment. Security is achieved through the use of a 16-bit CRC, a 16-bit CRC seed, a 96-bit device ID, and a 32-bit random challenge. The CRC polynomial, CRC seed, and 96-bit ID are unique from device to device, and are stored as encrypted text in public memory, and as plain text in private memory. The host system can decrypt the polynomial, seed, and ID values using a shared key that is stored in end-equipments memory. The encryption method and shared key used to store the polynomial coefficients and the device ID can be selected by the manufacturer. *Contact TI for information regarding specifics for encryption of the device ID and CRC polynomial coefficients.*

To authenticate a battery pack, the host reads the encrypted device ID, polynomial, and seed values. It decrypts those values, then generates a 32-bit random challenge, which is transmitted to the bq26150. The bq26150 uses the plain-text version of the polynomial coefficients and device ID, along with the 32-bit random challenge from the host, to calculate the authentication CRC value. The host uses the polynomial coefficients, seed, and device ID that it decrypted, along with the 32-bit random challenge it sent to the bq26150, to calculate the authentication CRC value. When the host and bq26150 have completed the calculations, the host can read the authentication CRC value the bq26150 computed and compare to its own value. If the values match, the battery pack is authenticated.

The bq26150 has a communication pass-through mode that allows it to be used in systems with an existing HDQ based battery monitor or gas gauge. Once the battery pack is authenticated, the bq26150 can be put in continuous pass-through mode, allowing the host system to communicate with a second HDQ device with no additional overhead. A one-time pass-through mode is also available, allowing the host to communicate once to the second HDQ device as needed.

The bq26150 obtains the power needed to run from the HDQ bus. An external capacitor is charged when the bus is high and discharges while the bus is low. If the bq26150 is not authenticating or communicating and the HDQ bus is low, the power is reduced and it enters sleep mode. If the bus is held low until the capacitor fully discharges, the bq26150 is disabled.

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APPLICATION INFORMATION (continued)

Register Interface

Table 1. Memory Map

HDQ ADDRESS	NAME	FUNCTION
NONVOLATILE REGISTERS		
0x7F – 0x70	GEN	General Purpose Memory
0x6F – 0x60	RSVD	Reserved
0x5F – 0x59	RSVD	Reserved
0x58	DL	Device Lock
0x57 – 0x51	RSVD	Reserved
0x50	SKI	Secret Key Index
0x4F – 0x4E	EDS	Encrypted polynomial seed (ES[15:0])
0x4D – 0x4C	EDP	Encrypted polynomial coefficients (EP[15:0])
0x4B – 0x48	EDK1	Encrypted device ID registers (EI[95:64])
0x47 – 0x40	EDK0	Encrypted device ID registers (EI[63:0])
0x3F – 0x3E	PDS	Plaintext polynomial seed(PS[15:0])
0x3D – 0x3C	PDP	Plaintext polynomial coefficients (PP[15:0])
0x3B – 0x38	PDK1	Plaintext device ID registers (PI[95:64])
0x37 – 0x30	PDK0	Plaintext device ID registers (PI[63:0])
RAM REGISTERS		
0x2F – 0x1A	RSVD	Reserved
0x19	FACTORY	Factory Reserved
0x18	CTRL	Authentication control register
0x17 – 0x06	RSVD	Reserved
0x05 – 0x04	AC	Authentication CRC value (AC[15:0])
0x03 – 0x00	RC	Random challenge registers (RC[31:0])

Memory Descriptions

Reserved Registers (RSVD)–Addresses 0x6F–0x59, 0x57–0x51, 0x2F–0x1A, 0x17–0x06

Registers reserved for future use. Any read from these registers returns 0xFF.

General Use (GEN) – Addresses 0x7F – 0x70

General use memory allows battery manufacturer or other pack information to be stored in nonvolatile memory.

Device Lock (DL) – Addresses 0x58

When DL[7:4] is nonzero, any attempt to write the EDS, EDP, EDK1, PDS, PDP, or PDK1 registers is blocked. When DL[3:0] is nonzero, any attempt to write to EDK0 or PDK0 is blocked. This feature allowed two entities to write device information, providing for more secure programming. The lock takes effect immediately after the DL register is written.

Secret Key Index (SKI) – Addresses 0x50

This non-volatile register can be used in the event that more than a single key is used by the host to decrypt the EDP and EDK registers. For example, multiple pack manufacturers may be utilized to assembly packs for the end equipment. Each pack manufacturer can be given a separate key (K_S), and key index value (I), to encrypt the plaintext polynomial and device ID values. The host end equipment is then programmed with each secret key (K_S) used by the various pack manufacturers. When authentication is attempted, the host reads the encrypted polynomial, device ID, and key index values. The K_S used by the manufacturer with key index is then selected to decrypt the values to plaintext.

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Encrypted Device Seed (EDS) – Addresses 0x4F – 0x4E

The unique 16-bit CRC seed stored as ciphertext in public nonvolatile memory. The host reads this seed and decrypts it using the shared key. The output of the decryption is the plaintext CRC seed that is used by the host to initialize the authentication CRC.

Encrypted Device Polynomial Coefficients (EDP) – Addresses 0x4D – 0x4C

The unique 16-bit CRC polynomial stored as ciphertext in public nonvolatile memory. The host reads this register pair and decrypts it using the shared key. The output of the decryption is the plaintext polynomial coefficients that are used by the host to define the authentication CRC.

Encrypted Device ID (EDK) – Addresses 0x4B – 0x40

The unique 96 bit device ID used stored as ciphertext in public nonvolatile memory. The host reads this register pair and decrypts it using the shared key. The output of the decryption is the plaintext device ID that are used by the host to define the authentication CRC.

Plaintext Device Seed (PDS) – Addresses 0x3F – 0x3E

The unique 16 bit CRC seed stored as plaintext in private non-volatile memory. The seed registers are written to the OTP at pack manufacturing or IC test. The plaintext seed is used by the bq26150 to initialize the authentication CRC. Any attempt to read the plaintext seed registers will return data 0xFF.

Plaintext Device Polynomial Coefficients (PDP) – Addresses 0x3D – 0x3C

The unique 16 bit CRC polynomial stored as plaintext in private nonvolatile memory. The coefficients are written to the OTP at pack manufacturing or IC test. The plaintext polynomial coefficients are used by the bq26150 to define the authentication CRC. Any attempt to read the plaintext polynomial coefficients returns data 0xFF.

Plaintext Device ID (PDK) – Addresses 0x3B – 0x30

The unique 96 bit device ID used stored as plaintext in public nonvolatile memory. The device is written to the OTP at pack manufacturing or IC test. The plaintext device ID is used by the bq26150 to calculate the authentication CRC value. Any attempt to read the plaintext device ID returns data 0xFF.

Factory Reserved (FACTORY) – Address 0x19

This register is used internally to TI for simple identification. Writes are not permitted, and reads return a random value.

Control Register (CTRL) – Address 0x18

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	CPASS	OPASS	RSVD	RSVD	RSVD	POR	DONE	AUTH
POR STATUS	0	0	0	0	0	1	0	0

CPASS   Writing the bit to a **1** enables the Continuous HDQ Pass Through mode. All communication then passes through the HDQP pin, allowing the host to reach a 2nd HDQ based device. The CPASS bit is cleared when the bq26150 detects three consecutive breaks.

OPASS   Writing this bit to a **1** enables the One Time HDQ Pass Through mode. The next 16 valid bits of communication passes through the HDQP pin, allowing the host to reach a 2nd HDQ based device. The OPASS bit is cleared following the 16th valid data bit or when three consecutive breaks are sent from the host.

RSVD   Reserved – These bits are available for future functions. These bits (5, 4, and 3) should be written to **0** when the host system writes to the control register. These bits always return a **0** when the host reads from the control register

POR   The POR bit is set to **1** by the bq26150 following a Power on Reset. This is a flag to the host that V_{CC} was less than $V_{(POR)}$ for some period of time. The device undergoes a full reset on a POR condition. The host must clear the bit. The host may set this bit, but it has no effect on the bq26150.

DONE   DONE is set when bq26150 has completed calculating the CRC after AUTH bit has been set. This is a flag to the host system that the message/authentication registers contain the calculated CRC value. The bit is automatically cleared when the AUTH bit is set.

AUTH   Writing this bit to **1** initiates the CRC calculation. The message written to the message/digest registers, 0x03 – 0x00, are used as input. This bit is automatically cleared when the CRC calculation is complete and the authentication value has been written to the message/authentication registers.

Authentication CRC Value (AC) – Addresses 0x05 – 0x04

The value computed from the CRC. The register is cleared on POR. This register cannot be written by the host system

Random Challenge (RC) – Addresses 0x03 – 0x00

The host system writes this register set with a random challenge that is used to calculate the CRC value (see below for details on the CRC calculation). The bq26150 uses the entire 4 bytes to calculate the CRC when the AUTH bit (CTRL[0]) is written to 1. After the authentication value is calculated, bq26150 writes the digest to the AC registers, clear the AUTH bit and set the DONE bit (CTRL[1]).

CRC Description

A CRC, or cyclic redundancy check, is normally used to detect small errors in the transmission of data. A CRC calculation is a form of polynomial modulo 2 arithmetic, so a CRC is usually referenced by means of a polynomial, i.e., $1 + x^4 + x^5 + x^{16}$. Most *correct* CRC polynomials ensure that the highest and lowest polynomial orders have a coefficient of 1. The highest order coefficient represents the number of bits in the final CRC value and the other terms with a coefficient of 1 represent the tap points where an XOR is performed. The example CRC $1 + x^4 + x^5 + x^{16}$ would then represent a 16 bit CRC value, with tap points at the x^5, x^4, and x^0 stages. The bq26150 uses a 16 bit type 2 linear feedback shift register with programmable tap points. This allows the CRC polynomial to vary from device to device.
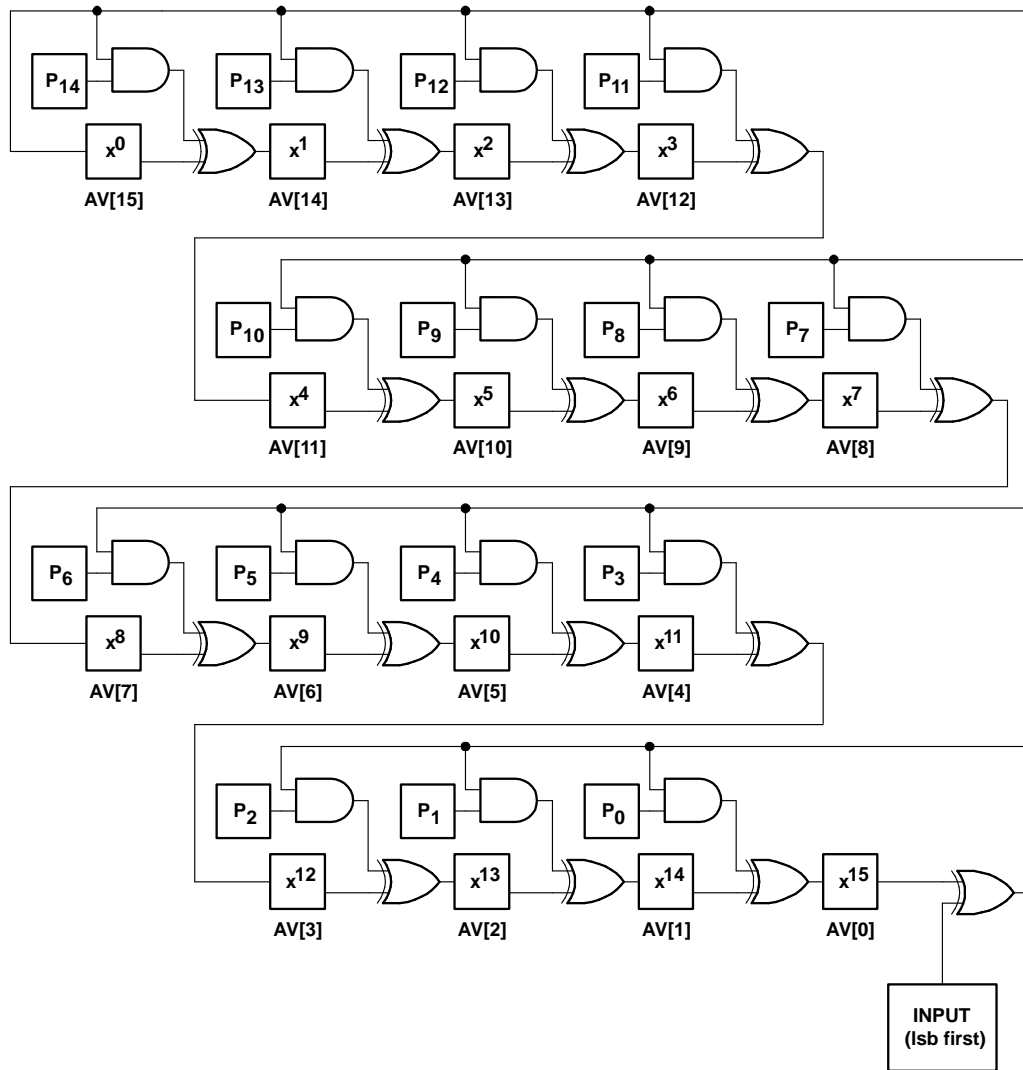
Figure 3. bq26150 Programmable CRC Hardware Implementation

The generic polynomial used in the bq26150 can be written as:

$$1+P_{14}x^1+P_{13}x^2+_{12}x^3+P_{11}x^4+P_{10}x^5+P_9x^6+P_8x^7+P_7x^8 P_6x^9+P_5x^{10}+_4x^{11}+P_3x^{12}+P_2x^{13}+P_1x^{14}+P_0x^{15}+x^{16}$$

Figure 3 shows the hardware implementation of the CRC, with the corresponding bits of the authentication value shown below each stage of the shift register. This configuration assumes that the x^0 term coefficient, which is P_{15}, is always 1, which was stated as an assumption of a *normal* CRC polynomial. This means that there are 2^{15}, or 32768, possible CRC polynomial values. In actually, the number of possible CRC polynomial will be less than 32758 because some values, such as all 0, do not provide sufficient mixing of the results to be secure.

To authenticate a battery pack using the bq26150, the host must reproduce the CRC calculation in software. This is done by reading the encrypted device ID and encrypted polynomial coefficients, and encrypted seed. All values are decrypted by the host to provide the 16-bit polynomial, 16-bit seed, and 96 of the 128 bits of calculation's input. The CRC input is:

Device ID [95:0]	Random Challenge [31:0]

Input MSB

Input LSB

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Figure 4 provides a pseudo-code example of calculating the CRC in software and Figure 5 shows an example of the CRC calculations inputs and associated output.

```
poly = P [15 : 0] ;
strcpy (input, key [ 63 : 0 ] ) ;
strcat (input, challenge [ 31 : 0 ] ) ;
for ( i = o ; i < 96 ; i + + )
{
    if (crc [ 0 ] ^ input [ i ] )
      crc = ( crc >> 1 ) ^ poly;
    else
      crc =  crc >> 1 ;
}
```

Figure 4. Pseudo-C Code for CRC Calculation

```
Polynomial = 1 + x² + x⁵ + x¹¹ + x¹⁶

P [ 15 : 0 ] = 1010010000010000        (binary)
             = A410                    (hex)


Seed [15:0] = 6a9f                     (hex)


Decrypted Device ID = 65a9b4f38dcc217d (hex)
Random Challenge = a0071d8e            (hex)

CRC input = a0071d8e65a9b4f38dcc217d  (hex)

CRC output = 7ef8
```

Figure 5. Example Inputs and Output of CRC Calculation

Writing and Reading Nonvolatile Memory

The bq26150 has sixteen bytes of nonvolatile one time programmable memory for general use and 32 bytes for authentication information that can be programmed by the HDQ engine. All OTP registers are cleared at final test, allowing for programming at pack manufacturing.

Programming a nonvolatile memory location requires sending the HDQ write command to that location and then pulling the HDQ line up to 7 V for 300 μs. If the programming pulse is not provided, the data transmitted by the host will not programmed into the OTP. Figure 6 shows an example of writing and programming address 0x71 with data 0x55 (*timings are not drawn to scale*). Figure 6, Figure 7 and Table 2 provide more information on the programming pulse specifications.
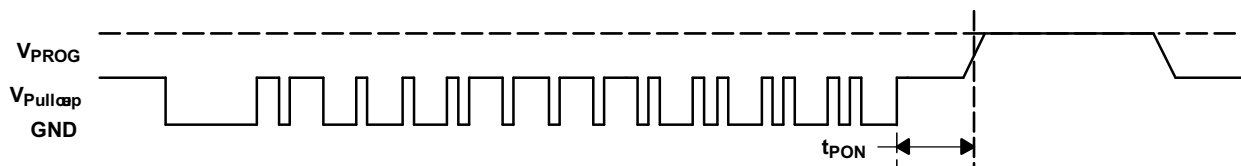
Figure 6. Writing and Programming OTP Example
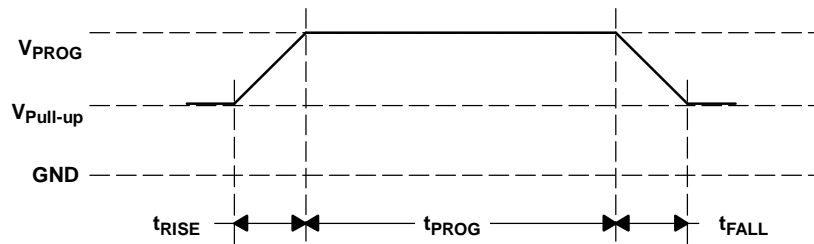
Figure 7. OTP Programming Pulse

Table 2. OTP Programming Specifications

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{PON}	Write to pulse rise		2		µs
t_{RISE}	Pulse rise time	No overshoot above 7.7 V	1	10	µs
t_{PROG}	Pulse high time		300		µs
t_{FALL}	Pulse fall time		1	10	µs

The nonvolatile memory can be written to more than once. However, the data already in the byte goes through a logical bitwise OR with the new data. For example, if address 0x71 was programmed with data 0x55 initially and a second program to address 0x71 with data 0xAA was performed, subsequent reads of address 0x71 would return data 0xFF (0x55 OR 0xAA = 0xFF).

Communication With a 2nd HDQ Device

The bq26150 has two communication pass through modes to allow communication to a second HDQ based device from Texas Instruments. These modes allow the bq26150 to be put in an existing system utilizing a bq2018, bq2019, bq262xx, or bq27xxx device. The pass through modes can be enabled by setting the CPASS or OPASS bits in the control register.

The Continuous Pass Through (CPT) mode is enabled when the CPASS bit is set. While in this mode the bq26150 passes all communication through to the 2nd device on the bus. The CPT mode is cancelled when the host transmits three consecutive breaks. Note that the 2nd device on the bus may only see two of these three breaks. The CPASS bit automatically clears after the third break is received.

The One Pass Through (OPT) mode is enabled when the OPASS bit is set. While in this mode, the bq26150 passes 16 valid HDQ bits. This allows the host to perform a single read or write to the 2nd HDQ device. The OPT mode is cleared after the 16th valid HDQ bit passes through the bq26150 or when 3 consecutive breaks are received from the host. Note that the 2nd HDQ device may only see two of these three breaks. The OPASS bit is automatically cleared after the 16th bit or the third break.

The OPT mode is useful for putting a 2nd HDQ device to sleep. The OPASS bit can be set in the bq26150, allowing the sleep command to be passed to the 2nd HDQ device. After the 16th bit is received from the host, communication reverts to the bq26150. The HDQP line will not be disturbed and the 2nd device enters sleep mode as expected.

If the host writes both the CPASS and OPASS bits, the CPASS bit has priority and remains set after the first pass through is completed. The OPASS bit is cleared.

Sending a Break During a Pass Through Read:

The bq26150 pass through mode is implemented in logic rather than connecting the HDQ/HDQP pads directly through an analog transmission gate. This means the bq26150 cannot transmit the first break it receives to the 2nd device while the data is being driven from the 2nd device to the master. To transmit a break to the 2nd device while it is transmitting, the host is required to send 2 breaks. The first resets the bq26150 engine and prepares it to transmit from the host to the 2nd device. The second break actually reaches the 2nd HDQ device.

Putting a bq262x0 to Sleep using Pass Through:

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A system using the bq26150 and a bq26200 or bq26220 communicates to the monitor during normal usage. This means that the continuous pass-through mode is used. To put the bq262x0 to sleep, the host should exit continuous pass through mode and put the bq26150 in one-time-pass-through mode. The host can then communicate to the bq262x0 to issue the sleep command and communication control reverts to the bq26150. The HDQP is not disturbed, allowing the bq262x0 to enter the low power mode. To wake the bq262x0, the bq26150 can be put in either continuous or one-time-pass-through mode and a break can be issued from the host.

Communicating With bq26150

The bq26150 includes a single-wire HDQ serial data interface. Host processors, configured for either polled or interrupt processing, can use the interface to access various bq26150 registers. The HDQ pin is an open drain device, which requires an external pull-up or pull-down resistor. The interface uses a command-based protocol, where the host processor sends a command byte to the bq26150. The command directs the bq26150 either to store the next eight bits of data received to a register specified by the command byte, or to output the eight bits of data from a register specified by the command byte.

The communication protocol is asynchronous return-to-one and is referenced to V_{SS}. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 5 Kbits/s. The least-significant bit of a command or data byte is transmitted first. Data input from the bq26150 may be sampled using the pulse-width capture timers available on some microcontrollers. A UART can also be configured to communicate with the bq26150.

If a communication time-out occurs, for example, if the host waits longer than $t_{(RSPS)}$ for the bq26150 to respond or if this is the first access command, then a BREAK should be sent by the host. The host may then re-send the command. The bq26150 detects a BREAK when the HDQ pin is driven to a logic-low state for a time $t_{(B)}$ or greater. The bq26150 is ready for a command from the host processor $t_{(BR)}$ seconds after the HDQ line is released from the break.

The return-to-one data-bit frame consists of three distinct sections:

1. The first section starts the transmission by either the host or the bq26150 taking the HDQ pin to a logic-low state for a period equal to $t_{(HW1)}$ or $t_{(DW1)}$.
2. The next section is the actual data transmission, where the data should be valid for $t_{(HW0)}$–$t_{(HW1)}$ or $t_{(DW0)}$–$t_{(DW1)}$.
3. The final section stops the transmission by returning the HDQ pin to a logic-high state and holding it high until the time from bit start to bit end is equal to $t_{(CYCH)}$ or $t_{(CYCD)}$.

The HDQ line may remain high for an indefinite period of time between each bit of address or between each bit of data on a write cycle. After the last bit of address is sent on a read cycle, the bq26150 starts outputting the data after $t_{(RSPS)}$ with timing as specified. The serial communication timing specification and illustration sections give the timings for data and break communication. Communication with the bq26150 always occurs with the least-significant bit being transmitted first.

Plugging in the battery pack may be seen as the start of a communication due to contact bounce. It is recommended that each communication or string of communications be proceeded by a break to reset the bq26150s HDQ engine.

Command Byte

The Command byte of the bq26150 consists of eight contiguous valid command bits. The command byte contains two fields: W/R Command and address. The Command byte values are shown in the following table:

7	6	5	4	3	2	1	0
W/R	AD6	AD5	AD4	AD3	AD2	AD1	AD0

W/R   Indicates whether the Command bytes is a read or write command. A **1** indicates a write command and that the following eight bits should be written to the register specified by the address field of the Command byte, while a **0** indicates that the command is a read. On a read command, the bq26150 outputs the requested register contents specified by the address field portion of the Command byte.

AD6–AD0   The seven bits labeled AD6–AD0 containing the address portion of the register to be accessed.

Cryptography Glossary

This glossary is not intended to be exhaustive, but provides a quick reference to some of the terms included in this document.

Plaintext

Data in an immediately usable form. *Texas Instruments Incorporated* is an example of a plaintext string.

Ciphertext

Data that has been encrypted with any of a number of cipher algorithms. If *bq26150* is the plaintext, the ciphertext string might be represented as *)d*0dsF.

Shared Secret Key

A key used by both Texas Instruments Incorporated and the host manufacturer to encrypt or decrypt the unique device ID. Contact the factory for more specific information.

Unique Device ID

A 96-bit value used to calculate the CRC authentication value.

Encrypted Polynomial Coefficients

Encrypted version of the 16-bit device specific CRC polynomial.

Encrypted Device ID

The encrypted version of the 96-bit unique device ID.

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
BQ26150DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
BQ26150DCKRG4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DCK (R−PDSO−G5)   PLASTIC SMALL−OUTLINE PACKAGE

2,15
1,85

5   4

1,40
1,10

2,40
1,80

Pin 1
Index Area   1   2   3

0,65

5X 0,30
    0,15

1,30

⊕ | 0,10 Ⓜ

0,22
0,08

Gauge Plane
Seating Plane

0,15   0°−8°

0,46
0,26

1,10
0,80

⌒ | 0,10

Seating Plane

0,10
0,00

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NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
        D. Falls within JEDEC MO−203 variation AA.

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